TITLE	DOC No. RFD-20250916100-001	
400G QSFP-DD SR8 AOC Transceivers	REVISION：01	AUTHORIZED BY：Hawk Rong
	DATE：2025.09.16	CLASSIFICATION ：Active Optical Cable

1. PRODUCT FEATURES

- Data rate up to 425Gb/s (8x PAM4 53Gb/s)
- 850nm VCSEL laser and PIN receiver
- High speed I/O electrical interface (400GAUI-8)
- I2C interface with integrated Digital Diagnostic Monitoring (DDM)
- Single +3.3V power supply
- Power consumption less than 10W per end
- Low latency time with DSP solution
- Operating case temperature:0~+70°C
- Compliant to RoHS-10

2. PRODUCT APPLICATIONS

- 400GBASE-SR8

3. PRODUCT DESCRIPTION

The 400Gb/s QSFP-DD active optical cable (AOC).It is compliant with the QSFP-DD MSA Rev5.0 and IEEE 802.3bs, IEEE802.3cm, and Common Management Interface Specification Rev4.0. The 400G AOC is an assembly of eight full-duplex lanes, where each lane is capable of transmitting data at rates up to 53.125Gb/s PAM-4 signal mode.

3.1 PRODUCT NAME AND SERIES NUMBER(S)

400G QSFP-DD SR8 Active Optical Cable

Bit Rate	Laser(nm)	Distance	Fiber Type	Connector	Tem.
400G QSFP-DD AOC	850nm	1~100m	MMF	N/A	C

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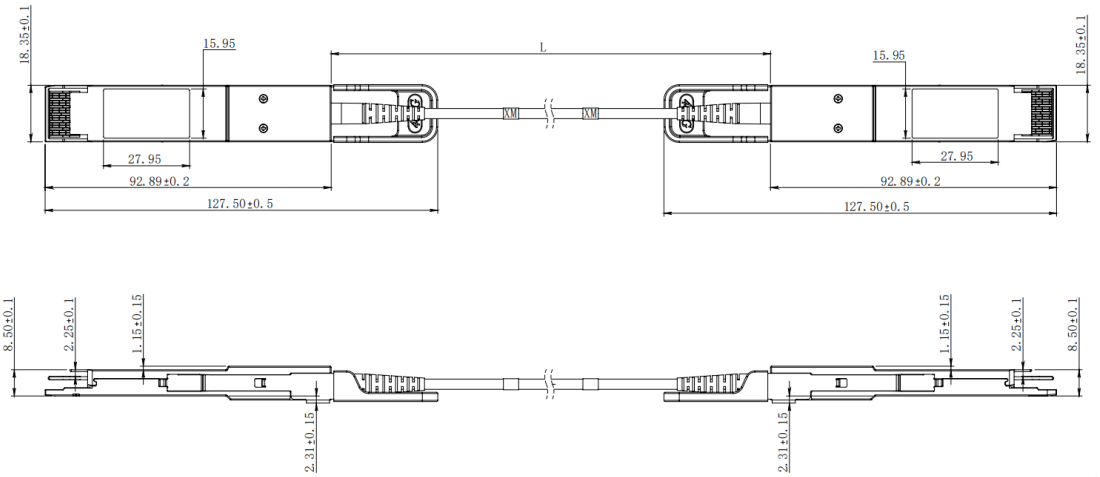
3.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Unit is millimeter. All dimensions are ±0.1mm unless otherwise specified

4. AbsoluteMaximum Ratings(TC=25°C, UNLESS OTHERWISE NOTED)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+85	ºC	
Maximum Supply Voltage	Vcc	-0.5	-	4.0	V	
Operating Relative Humidity	RH	15	-	+85	%	

5. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case temperature	Tc	0	-	+70	ºC	
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Power Supply Current	Icc	-	-	3	A	
Power Consumption (per end)		-	-	10	W	
Data Rate (per lane)		-	53.125	-	Gb/s	

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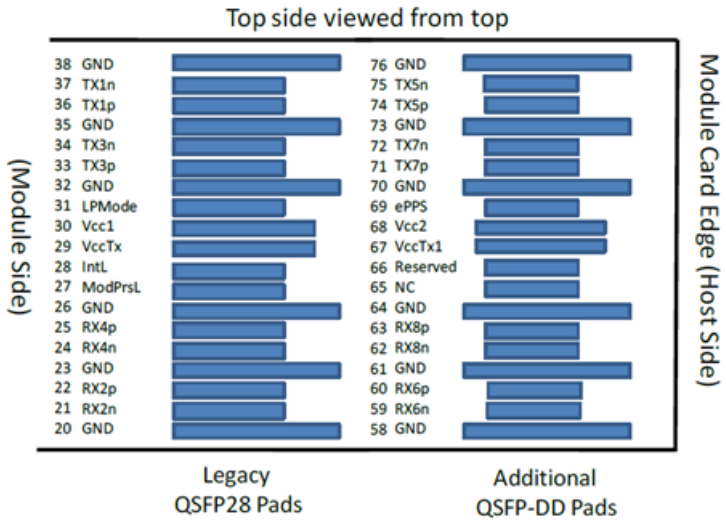
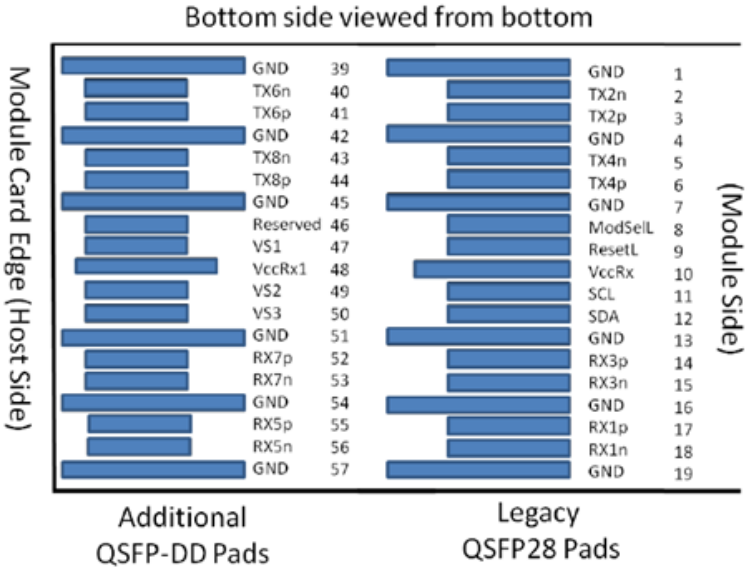
6. Applications Note:

Pin Definitions





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Pin Function Definitions

Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

[1] QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B (see Figure 2 for pad locations). Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A, 3B.

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7. Data Rate Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Bit Rate (per lane)	BR		53.125		Gb/s	
Electrical Bit Error Rate (per lane)	BER			2.4E-4		Notes

Notes: PRBS31Q@26.5625GBd. Pre-FEC

8. Low Speed Control And Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 45
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 45.
LPMode, ResetL, ModSelL and ePPS	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	uA	0V<Vin<Vcc
ePPS	|Iin|		TBD	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	VCC-0.5	VCC+0.3	V	10k Ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

9. Digital Diagnotic Specifications

Parameter	Symbol	Min	Max	Units	Notes
Transceiver case temperature accuracy	DMI_TEMP	-5	+5	℃	Over operating temp
Supply voltage monitor accuracy	DMI _VCC	-3%	+3%	V	Full operating range
Channel Bias current monitor accuracy	DMI_IBIAS	-10%	+10%	mA	Per channel

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Channel RX power monitor absolute error	DMI_RX	-3	3	dB	Per channel
Channel TX power monitor absolute error	DMI_TX	-3	3	dB	Per channel
DDM TX Power	DDM_TX_ Power	-6.2		dBm	Per channel
DDM RX Power	DDM_RX_ Power	-6.2		dBm	Per channel

10. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2025.09.16	Hawk Rong	Mike Sun